



HARDWARE

REFERENCE DESIGN

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UFirebird IV - UC7510

Multi-GNSS Single-Frequency
Positioning Chip

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Foreword

About This Document

This manual provides the schematic diagrams, hardware design considerations, and recommended BOM for the Unicore UC7510 chip.

Target Readers

This manual is intended for technical personnel familiar with GNSS receivers.

Statement

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Revision History

Version	Revision History	Date
R1.0	First release.	Feb. 2026

Document Status

Releases	Status Descriptions	Current Status
Primary	This is a pre-release version with target specifications that are subject to revision.	
Alpha release	This is an alpha release version, which has been preliminarily tested and verified. The content may undergo minor modifications based on user feedback and further testing.	
Production release	The document contains the complete and final specifications.	✓

1 Reference Design

The reference circuit for the UC7510 chip is shown below. When conducting hardware design, please pay attention to the followings:

- V_CORE and V_RF use the same power supply.
- The external TCXO is powered through the LDO_X pin.
- Connect an external RTC crystal.
- Connect an external LNA and SAW filter.
- Use the UART interface for communication.

Caution:

- RTC and backup function are the prerequisites of GNSS hot start. If they are not used, the V_BACK pin needs to be connected to ground or V_IO.
- It is recommended to design an independent power rail for the antenna to reduce the risk of damage to the chip. If the antenna's power supply and the chip's main power supply use the same power rail, the ESD, surge and overvoltage introduced at the antenna will be directly applied to the main power supply, which may cause damage to the chip.

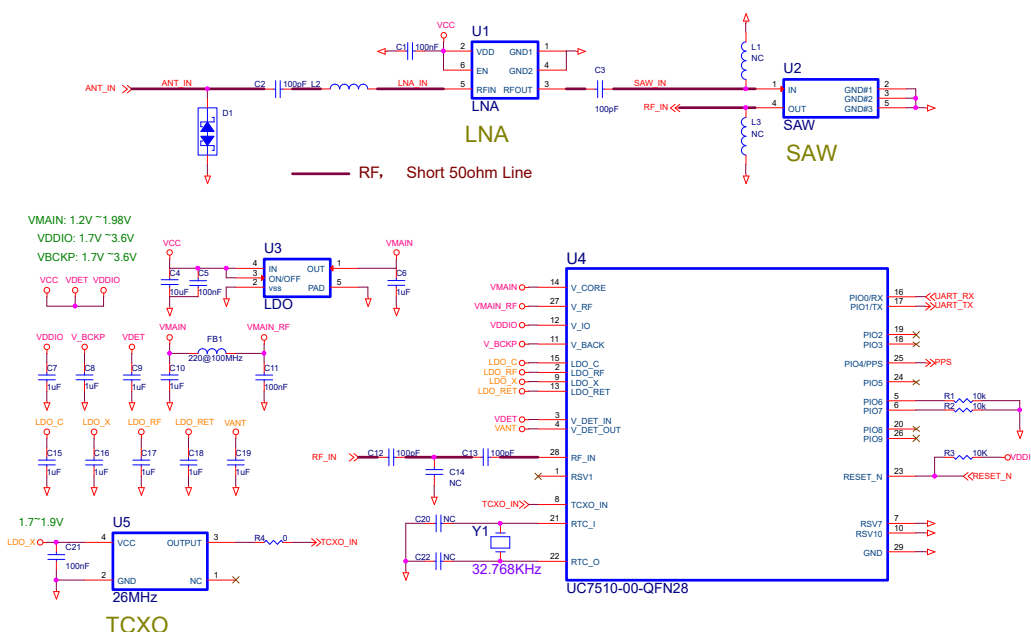


Figure 1-1 Schematic Diagram

2 Attention

2.1 Power

For all the power supplies, the ripple voltages must not exceed 50 mV.

In order to avoid the impact of uncontrollable factors and ensure the stability of the chip, it is recommended that the power supply of UC7510 can control the chip's power on and off to restore the system.

V_CORE/V_RF

- V_CORE and V_RF must use the same power supply, and V_RF needs a ferrite bead to filter noise.
- The initial level of V_CORE and V_RF when powered on needs to be less than 0.4 V.
- The power-on ramp of V_CORE and V_RF needs to be monotonic, without plateaus.
- The undershoot and ringing of V_CORE and V_RF when powered on need to be within 5% of the supply voltage.
- Power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μ s ~ 10 ms.
- Power-on time interval: The time interval between the power-off (< 0.4 V) to the next power-on needs to be larger than 100 ms.

V_IO

- V_IO needs to be powered no later than V_CORE/V_RF.
- The initial level of V_IO when powered on needs to be less than 0.4 V.
- The power-on ramp of V_IO needs to be monotonic, without plateaus.
- The undershoot and ringing of V_IO when powered on need to be within 5% of the supply voltage.
- Power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μ s ~ 10 ms.
- Power-on time interval: The time interval between the power-off (< 0.4 V) to the next power-on needs to be larger than 100 ms.

V_BACK

- The initial level of V_BACK when powered on needs to be less than 0.4 V.
- The power-on ramp of V_BACK needs to be monotonic, without plateaus.
- The undershoot and ringing of V_BACK when powered on need to be within 5% of the supply voltage.
- Power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μ s ~ 10 ms.
- Power-on time interval: The time interval between the power-off (< 0.4 V) to the next power-on needs to be larger than 100 ms.
- V_BACK shall not be floating. When RTC time keeping mode is not used, V_BACK must be connected to ground or V_IO.

2.2 Reset

UC7510 supports system reset. The reset signal is active low and the active time needs to be no less than 1 ms.

2.3 RTC

RTC is usually driven by an on-chip 32768 Hz oscillator, which needs to be connected to an external 32768 Hz crystal. It supports two kinds of connections:

1. Use an external crystal, as shown in the schematic diagrams.
2. Use an external 32768 Hz digital clock signal to directly input to the RTC_I pin, and the RTC_O pin needs to be floating. The clock error is required to be no more than $\pm 0.6\text{Hz}/\pm 20\text{ppm}$.

Attention: When using an external digital clock signal, it is recommended to do ESD protection at the RTC_I pin, and ensure that the signal amplitude must be within 2 V to MIN (V_IO, V_BACK)¹, otherwise the chip may be permanently damaged.

When RTC is not used, connect RTC_I to ground and leave RTC_O floating.

In addition to the general rules of RTC layout and routing, please pay special attentions to the followings:

- Ensure complete GND under the chip and the RTC crystal.
- Place the RTC crystal as close to the chip as possible, and DO NOT place other devices between them.

- Avoid placing any high-power or strong-interference devices, signals, traces, etc. around the RTC crystal.
 - It is recommended to implement ground shielding for the RTC circuits.
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¹The voltages of V_IO and V_BACK must be larger than 2 V.

2.4 TCXO

The TXCO_IN pin is used for connecting an external TCXO of 26 MHz. The TCXO can be powered by LDO_X or an external independent LDO. When V_IO is 1.8 V, use an external independent LDO to power the TCXO.

In order to ensure the chip boots normally, the 26 MHz clock is required to work stably within 10 ms after the chip is powered.

The basic parameters of TCXO are as follows:

- Frequency: 26 MHz $\pm$ 0.5 ppm (within all the temperature ranges);
- Short-term frequency stability: < 5 ppb/s.

In addition to the general rules of TCXO layout and routing, please pay special attentions to the followings:

- In order to reduce the impact of heat conduction on the performance of TCXO, it is recommended to maintain the copper void for the layer where the TCXO is placed and its adjacent layers, and keep the reference ground complete for other layers.
- Place the TCXO away from any heat source or interference source, with ground shielding for the surrounding circuits.
- Avoid placing any high-power or strong-interference devices, signals, traces, etc. around the TCXO. Keep a distance of more than 3 times the trace width between the clock trace and other traces.

3 Recommended BOM

Table 3-1 Recommended BOM

Category	Symbol	Description	Model	Manufacturer
10uF capacitor	C4	0402 surface mount capacitor, 10uF $\pm$ 20% X6S 6.3V	CM05 X6S10 6M06 AH	KYOCERA
1uF capacitor	C6 C7 C8 C9 C10 C15 C16 C17 C18 C19	0201 surface mount capacitor, 1uF $\pm$ 20% X6S 6.3V	CM03 X6S10 5M06 AH039	KYOCERA
100nF capacitor	C1 C5 C11 C21	0201 surface mount capacitor, 100nF $\pm$ 10% X7S 10V	GRM0 33C71 A104K E14D	Murata
100pF capacitor	C2 C3 C12 C13	0201 surface mount capacitor, 100 pF $\pm$ 10% X7R 25 V	CC020 1KRX7 R8BB1 01	YAGEO
TVS	D1	ESD protective diode, DFN0603-2L 1100 W $\pm$ 18 kV	JEB05 UCDS- AH	JIEJIE MICROELECTRONICS CO., Ltd
Ferrite bead	FB1	Ferrite bead, BLM15AG221SN1D	BLM1 5AG22 1SN1 D	Murata
10 k Ω resistor	R1 R2 R3	0201 surface mount resistor, 10 k Ω , 1/20 W, $\pm$ 1%	RC020 1FR-0 710KL	YAGEO
0 k Ω resistor	R4	0201 surface mount resistor, 0 Ω <50m Ω 1/20W	RC020 1FR-0 70RL	YAGEO
LNA	U1	LNA, Gain=18.5dB, NF=0.6dB, LGA 6-pin	MXDL N16GF	MAXSCEND

Category	Symbol	Description	Model	Manufacturer
SAW	U2	SAW filter, 1582.4MHz, 48.5MHz, 1.4mmx1.1mm	HDF15 88U-B 2	HD
LDO	U3	LDO, 300mA, XTDFN- 1×1-4L, 1x1x0.4mm	SGM2 036S- 1.8XX DH4G/ TR	SGMICRO
TCXO	U5	±0.5 ppm, 26 MHz, 2.0mm*1.6mm*0.61mm	X1G00 53710 20016	EPSON
Crystal	Y1	32.768 KHz, ±20 ppm, 12.5 pF	X1A00 01710 00118	EPSON

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